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Title of the Invention: IMAGE DISPLAY DEVICE

Specification

1. Title of the Invention IMAGE DISPLAY DEVICE

2. Claims

(1) In an image display device wherein pixel electrodes are arranged in a matrix on a semiconductor layer formed on an insulation substrate of glass and the like or on a semiconductor substrate, and a transparent electrode on a translucent substrate, mounted above the pixel electrodes with liquid crystal interposed therebetween, is made as an opposite electrode, the image display device characterized by comprising at least two switching elements and a one bit memory cell provided for one of the pixel electrodes.

(2) The image display device as claimed in claim 1 characterized in that each of input terminals of the two switching elements is connected in a one to one relationship to each of two signal lines to which signals with polarities thereof opposite to each other are applied, respectively.

(3) The image display device as claimed in claim 1 or claim 2 characterized by comprising means for selecting between an AC voltage waveform applied state and a no voltage applied state according to an output of the memory cell.

3. Detailed Description of the Invention

The present invention relates to an improvement of a fine dot image display device using liquid crystal.

A conventional image display device is shown in Fig. 1. The device is formed by combining liquid crystal with a MOSFET array. In Fig. 1, a unit pixel is formed by a MOSFET 1 formed in a semiconductor layer, a signal storing capacitor 2, and a liquid crystal cell 3. A basic operation of the device will be explained. First, the MOSFET is taken as that of a P channel and a negative pulse voltage as a gate signal is applied to a gate line xi. This makes the FET 1 in a turned-ON state to allow an image signal applied to a signal line yi to charge the capacitor 2 through the FET 1. When the negative pulse disappears, the FET 1 is brought into a turned-OFF state and a voltage charged in the capacitor 2 is held while being discharged through the liquid crystal cell and OFF-resistance of the FET to be continuously applied to the liquid crystal. Furthermore, the gate signals are line sequentially scanned from xi to $xi+_1$, $xi+_2$, ..., and image signals corresponding to positions thereof are applied to signal lines yi, $yi+_1$, ..., by which a whole image is displayed. At this time, the opposite electrode is a common transparent electrode affixed on the whole surface of the glass or the like, and reference numeral 4 in Fig. 1 denotes a common electrode terminal. Moreover, the

common electrode is always kept at a certain potential. Incidentally, although such an image display device is best suited for displaying an image including half-tone or a moving image, that is, a display of a television image, it is extremely unsuitable for displaying an image necessitating no half-tone or a still image. The reason for this is that a signal charged in the capacitor 2 is discharged through the liquid crystal cell 3 as explained before to rapidly lower the voltage across the capacitor unless a writing operation is always carried out, causing the voltage applied to the liquid crystal to change. This necessitates always carrying out a writing operation even in the case where a still image is displayed, which requires electric power for always activating the whole circuit. For example, in order to carry out writing of a picture with 200 x 200 pixels at a rate of 60 pictures per second, a maximum frequency of approximately 2.5MHz is necessary, which results in a considerably large amount of power consumption. Writing 60 pictures per second is a value necessary for AC driving of the liquid crystal without generating any flicker. Moreover, it is necessary to feed an electric current to the signal line for charging the capacitor, which results in a defect of causing inevitable increase in power consumption therefor.

Accordingly, it is an object of the present invention to provide an image display device which is suited for displaying an image necessitating no half-tone and a still image with a small amount of power consumption.

In the following, explanations of the invention will be carried out with drawings. Figure 2 shows an image display device according to the invention. A unit pixel is formed by

switching transistors 5 and 6, a memory cell 7, a signal selection circuit 8, and a liquid crystal cell 9. In addition, a clock source 10 is provided for AC driving of the liquid crystal. Here, the switching transistors 5 and 6 are formed by MOS transistors. Furthermore, the memory cell 7 is formed by a flip-flop. Assuming that a signal with a high voltage level is "1" and a signal with a low voltage level is "0", the flip-flop has an output set to be "1" (or "0") when a signal of "1" is inputted. The output is held in a previous state until next "0" signal is inputted. When a signal of "0" is inputted, the flip-flop has an output set to be "0" (or "1") and the state is maintained. In addition, the memory cell 7 is provided with two input terminals, a positive input terminal 7a that sets the output to be "1" when the input is "1" and a negative output terminal 7b that sets the output to be "1" when the input is "0". Further, the signal selection circuit 8 has an input to which a signal of the clock source 10 is inputted and, with the output of the memory cell 7 taken as a control signal, selectively outputs a signal in phase with the input signal and a signal in opposite phase with the input signal. An output of the signal selection circuit 8 is connected to a pixel electrode 9a. Moreover, sources of the switching transistors 5 and 6 are connected to signal lines yi and $\overline{yi}$ having polarities opposite to each other, respectively, and drains are connected to the positive input terminal 7a and the negative input terminal 7b of the memory cell 7, respectively. Now, an operation will be explained with the case taken as an example in which an output of the clock source 10 is connected to a common electrode terminal 11, an output and an input of the signal selection circuit 8

are made in opposite phase with each other when an output of the memory cell 7 is "1", and the output and the input of the signal selection circuit 8 are made in phase with each other when the output of the memory cell 7 is "0". First, when a negative pulse is applied to the gate line xi as a gate signal, the switching transistors (hereinafter abbreviated as s.Tr) 5 and 6 are brought into a turned-ON state to input items of image information applied to the signal lines yi and yi to the positive input terminal 7a and the negative input terminal 7b of the memory cell 7 through the s.Trs 5 and 6, respectively. Thus, an output of the memory cell 7 is set to be "1" or "0" according to the items of image information. When the gate signal disappears, the s.Trs 5 and 6 are brought into a turned-OFF state to make the memory cell keep holding the item of image information of "1" or "0" until a new item of image information is inputted. Therefore, until new items of information are written, all of the pixels keep holding items of image information being held at present however long the duration is. Moreover, in a pixel with an output of the memory cell being "1", the input and the output of the signal selection circuit 8 become in opposite phase with each other. Therefore, assuming that a power source voltage is V, a waveform of the clock source, that is, the common electrode potential and an output of the signal selection circuit, that is, the waveform of the pixel electrode become clocks in opposite phase with each other as denoted by 12a and 12b in Fig. 3A, respectively, by which an AC voltage 13a of ±V is applied to the liquid crystal 9 to make the pixel a selected pixel. Meanwhile, in a pixel with an output of the memory cell being "0", like in the above,

clocks in phase with each other are provided as denoted by 12a and 12c in Fig. 3B. Hence, no voltage is applied to the liquid crystal 9 at all as denoted by 13b to make the pixel a non-selected pixel. Therefore, it becomes possible to display an image without half-tone and the still image thereof with considerably low power. This is because all of driving circuits of the signal lines yi, $\overline{yi}$, $yi+_1$, $yi+_1$ ... and the gate lines xi, $xi+_1$ ... can be deactivated only with activation of the clock source 10, and the frequency of the clock source 10 is normally on the order of 30Hz, which brings consumed power to approximately zero. Moreover, the system is basically that of controlling the output of the memory cell without flowing current rather than that of charging a capacitor with a signal. This necessitates no current flowing in the signal lines at all, which also reduces consumed power considerably. The system is further the one which applies the clock also to the common electrode side. Therefore, assuming that the power source voltage is V, ±V, that is, an AC waveform with 2V of peak to peak can be applied to the liquid crystal to make it possible to lower the power source voltage compared with the voltage applied to the liquid crystal. This also makes it possible to achieve reduction in the consumed power. In addition, the display without half-tone allows all of peripheral driving circuits and image information processing circuits to be formed with CMOSs to thereby make it possible to also considerably reduce consumed power in the whole system. Meanwhile, the image signals, being inputted to the memory cell via the two paths of the signal line yi and the s.Tr 5, and the signal line yi and the s.Tr 6, allow redundancy of the signal paths to become

two times. This makes it possible to significantly reduce failure rate of the image due to breakage of the signal lines yi and $\overline{yi}$, and failure of the s.Trs 5 and 6 to considerably enhance yield of the display device.

A specific example of the image display device according to the invention is shown in Fig. 4. Namely, inverters 14 and 15 are used for the flip-flop for the memory cell with input and output terminals of the respective inverters 14 and 15 connected to each other, the input of the inverter 14 is taken as a positive input of the memory cell and connected to the s.Tr 5, the input of the inverter 15 is taken as a negative input of the memory cell and connected to the s.Tr 6, and the output of the inverter 15 is further taken as an output of the memory cell. Moreover, an exclusive-OR (hereinafter abbreviated as EOR) 16 is used as the signal selection circuit, the output of the above-described inverter 15, that is, the output of the memory cell, is taken as one input of the EOR circuit 16, and the output of the clock source 10 is taken as the other input of the EOR circuit 16. Furthermore, the output of the EOR circuit 16 is to be connected to the pixel electrode 9a. By such an arrangement, when "1" is set in the memory cell, an AC voltage ±V is applied to the liquid crystal, while, when "0" is set in the memory cell, no voltage is made to be applied to the liquid crystal at all, by which entirely the same operation as that explained with reference to Fig. 2 can be carried out. Here, from the view point of reducing the consumed power, CMOS inverters are desirably used for the inverters 14 and 15. In Fig. 5, another example of the image display device according to the invention. This is an example of using two transmission

gates (hereinafter abbreviated as TG) 17 and 18 as the signal selection circuit. With the memory cell formed with the inverters 14 and 15 in the same way as that in the example shown in Fig. 4, the output of the memory cell, that is, the output of the inverter 15, is connected to the n-channel side gate of the TG 17, the P-channel side gate of the TG 18, and the P-channel side gate of the TG 18. The input terminal of the inverter 15 is connected to the P-channel side gate of the TG 17 and the n-channel side gate of the TG 18. Moreover, the outputs of the TGs 17 and 18 are connected to the pixel electrode 9a with the outputs connected to each other, and the input terminal of the TG 18 is connected to the clock source 10 while being connected to the common electrode made common to all of the pixels. Furthermore, the input terminal of the TG 17 is connected to the clock source 10 through an inverter 19 while being made common to all of the pixels. Such arrangement makes the TG 17 in a turned-ON state and the TG 18 in a turned-OFF state when the output of the memory cell is "1" to allow an AC voltage of ±V to be applied to the liquid crystal cell as shown in Fig. 3A. In the same way, when the output of the memory cell is "0", no voltage is applied to the liquid crystal cell. In Fig. 6, there is shown further another example of the image display device according to the invention. There are used TGs 20 and 21 as the s.Trs. By using the TGs as the s.Trs, even when the power source voltage is lowered, the signals "1" and "0" can be surely transmitted. This makes it possible to enhance yield of the display device with redundancy of the signal path doubled even with reduced power source voltage.

In the examples shown in Fig. 4, Fig. 5, and Fig. 6, as

the signal selection circuit, the EOR circuit or two TGs are used. In effect, it is necessary only that the phase of the AC waveform applied to the pixel electrode can be made inverted when the output of the memory cell is provided as "1" and when provided as "0". Entirely the same operation can be provided by a combination of AND circuits or a combination of OR circuits. Thus, this is of course in the scope of the invention. Moreover, an arrangement of a circuit by which an AC voltage of ±V is applied when the output of the memory cell is "0" also provides entirely the same operation. Thus the explanation thereof will be omitted.

With the use of the image display device according to the invention as above, there can be completely accomplished the original object of obtaining an image display device which is suited for the display of an image necessitating no half-tone and a still image thereof, and requires only a small amount of consumed power. Namely, with an arrangement of a circuit being entirely digitized and all of peripheral circuits made turned-OFF except a clock source of the order of 30Hz when displaying a still image, considerable reduction in consumed power can be achieved. In addition, an AC driving, being made possible regardless of whether the images are still images or moving images, allows the display device to be obtained as being excellent also in life and reliability. Furthermore, the two signal paths provided in parallel can considerably enhance yield of the display device. Therefore, by applying the invention to a fine dot character display device and a fine dot graphic display device, a beautiful display, lowered consumed power, a long life, high reliability and a high yield can be achieved

at the same time to provide large industrial importance for the invention.

4. Brief Description of the Drawings

Figure 1 is a circuit diagram showing a conventional image display device; Figure 2 is a circuit diagram showing an image display device according to the invention; Figures 3(A) and (B) are explanatory diagrams showing liquid crystal driving voltages in the image display device according to the invention; Figure 4 is a circuit diagram showing a specific example of the image display device according to the invention; Figure 5 is a circuit diagram showing another specific example of the image display device according to the invention; and Figure 6 is a circuit diagram showing further another specific example of the image display device according to the invention.

5, 6 .. switching transistor, 7 .. memory cell, 8 .. signal selection circuit, 9 .. liquid crystal cell, 10 .. clock source, 11 .. common electrode terminal, 12a, 12b, 12c .. clock waveform, 13a, 13b .. liquid crystal driving voltage waveform, 14, 15 .. inverter, 16 .. exclusive-OR, 17, 18, 20, 21 .. transmission gate, 19 .. inverter.